APPENDIX A

1-48 (Cancelled).

49 (Previously Presented). A transmit circuit comprising:

a transmit data storage element configured to receive data from a transmit data input and sequentially transmit a transmit data output signal when the transmit circuit is operating in a normal mode, the transmit data storage element further configured to provide a repeating pattern signal when the transmit circuit is operating in a test mode, the transmit circuit sequentially transmitting the transmit data output signal based on the repeating pattern signal when the transmit circuit is operating in the test mode, wherein the transmit data storage element is loaded from the transmit data input to initialize the test mode.

50 (Original). The transmit circuit of claim 49 wherein the transmit data storage element comprises a shift register.

51 (Original). The transmit circuit of claim 49 further comprising:

a test loop coupled to the transmit data storage element when the transmit circuit is operating in the test mode, the

test loop providing feedback to allow the transmit data storage element to provide the repeating pattern signal.

52 (Original). The transmit circuit of claim 49 wherein the repeating pattern signal has a data length greater than a data capacity of the transmit data storage element.

53 (Original). The transmit circuit of claim 49 wherein the repeating pattern signal represents a sequence of data bits, the transmit data storage element storing each of the data bits.

54 (Original). The transmit circuit of claim 49 wherein, when the transmit data storage element is divided into transmit data storage sub-elements during operation in the normal mode, the transmit data storage sub-elements are combined as the transmit data storage element for providing the repeating pattern signal when the transmit circuit is operating in the test mode.

55 (Cancelled).

56 (Cancelled).

57 (Original). The transmit circuit of claim 49 wherein the

transmit data storage element is loaded via a parallel transmit load input.

58 (Currently Amended). The transmit circuit of claim 49 wherein the transmit circuit receives an adjustment signal from a receiver circuit, the receive circuit receiving the transmit data output signal, the transmit circuit adjusting a parameter of the transmit data output signal based on the adjustment signal.

59 (Original). The transmit circuit of claim 58 wherein the receive circuit is embodied in a first memory device and a second receive circuit is embodied in a second memory device.

60 (Original). The transmit circuit of claim 59 wherein the transmit circuit adjusts the parameter to a first value for communication with the first memory device and to a second value for communication with the second memory device.

61-76 (Cancelled).

77 (Previously Presented). A method for operating a transmit circuit to provide for evaluation of a digital signaling system

comprising the steps of:

passing transmit data through the transmit circuit when the transmit circuit is operating in a normal mode; and

generating a transmit repeating pattern in the transmit circuit when the transmit circuit is operating in a test mode by uniting a plurality of pipeline structures within the transmit circuit into a transmit repeating pattern generator when the transmit circuit is operating in the test mode.

78 (Original). The method of claim 77 wherein the step of generating a transmit repeating pattern in the transmit circuit further comprises the step of:

preloading an initialization pattern into the transmit circuit.

79 (Cancelled).

80 (Previously Presented). The method of claim 77 wherein the step of passing transmit data through the transmit circuit further comprises the step of:

passing distinct data through each of the plurality of pipeline structures when the transmit circuit is operating in the normal mode.

81 (Previously Presented). The method of claim 77 further comprising the steps of:

receiving the transmit data in a receive circuit when the transmit circuit is operating in the normal mode; and

receiving the transmit repeating pattern in the receive circuit when the transmit circuit is operating in the test mode.

82 (Previously Presented). The method of claim 77 further comprising the steps of:

receiving the transmit data in a receive circuit when the transmit circuit is operating in the normal mode; and

receiving the transmit repeating pattern in a test receiver separate from the receive circuit when the transmit circuit is operating in the test mode.

83 (Previously Presented). A method for operating a receive circuit to provide for evaluation of a digital signaling system comprising the steps of:

passing receive data through the receive circuit when the receive circuit is operating in a normal mode; and

generating a receive repeating pattern in the receive circuit when the receive circuit is operating in a test mode by

uniting a plurality of pipeline structures within the receive circuit into a receive repeating pattern generator when the receive circuit is operating in the test mode.

84 (Original). The method of claim 83 wherein the step of generating a receive repeating pattern in the receive circuit further comprises the step of:

preloading an initialization pattern into the receive circuit.

85 (Cancelled).

86 (Previously Presented). The method of claim 83 wherein the step of passing receive data through the receive circuit further comprises the step of:

passing distinct data through each of the plurality of pipeline structures when the receive circuit is operating in the normal mode.

87 (Previously Presented). The method of claim 83 further comprising the steps of:

transmitting the receive data to the receive circuit from a transmit circuit when the receive circuit is operating in the

normal mode; and

transmitting a transmit repeating pattern to the receive circuit from the transmit circuit when the receive circuit is operating in the test mode.

88 (Previously Presented). The method of claim 83 further comprising the steps of:

transmitting the receive data to the receive circuit from a transmit circuit when the receive circuit is operating in the normal mode; and

transmitting a transmit repeating pattern to the receive circuit from a test transmitter separate from the transmit circuit when the receive circuit is operating in the test mode.

89 (Cancelled).

90 (Previously Presented). A transmit circuit comprising:

a transmit data storage element configured to receive parallel data from a transmit data input and sequentially transmit a serial transmit data output signal when the transmit circuit is operating in a normal mode, the transmit data storage element further configured to provide a repeating pattern signal when the transmit circuit is operating in a test mode, the

transmit circuit sequentially transmitting the serial transmit data output signal based on the repeating pattern signal when the transmit circuit is operating in the test mode, wherein the transmit data storage element is loaded from the transmit data input to initialize the test mode.

91 (Cancelled).

92 (Previously Presented). A receive circuit comprising:

a receive data storage element configured to output a parallel receive data output signal based on a serial receive data input signal received at a receive data input when the receive circuit is operating in a normal mode, the receive data storage element further configured to provide a repeating pattern signal when the receive circuit is operating in a test mode; and

a comparison element configured to perform a comparison of a relationship between the repeating pattern signal and the serial receive data input signal received at the receive data input and to produce a comparison output signal based on the comparison when the receive circuit is operating in the test mode;

wherein the receive data storage element is loaded from the

receive data input to initialize the test mode.

93 (Cancelled).